UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,053	03/19/2004	Mitsuhiro Ichijo	740756-2718	7738

22204 7590 02/23/2007

NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,053	ICHIJO ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/28/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13-36,38-44,46-67,69-76,78 and 79* is/are pending in the application.

4a) Of the above claim(s) *16-33 and 47-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13-15,34-36,38-44,46,63-67,69-76,78 and 79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7, 15, 34, 39, 63, and 72 and 2-3, 5-6, 8-11, 13-14, 35-36, 38, 40-44, 46, 64-67, 69-71, 73-76, and 78-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US patent 6,781,162) in combination with Kihira et al. (US patent 6,631,022) and Fukui et al. (US patent 5,755,938) and **Danek et al. (US pub 2004/0099215) (a newly cited reference)**.

With respect to claims 1, 7, 8, 9, 13, 34, 39, 40, 41 , 42, 63, 64, 65, 72, 73, 74, 69, and 78, Yamazaki et al. teach a film formation method comprising the steps of (see col. 26, lines 1-30 and associated figures):

forming a first film (target silicon nitride) on internal portions of a chamber 113 ;

installing a substrate into the chamber after forming the first film; and

forming a silicon nitride protective film is formed over a surface of the substrate by using the first film and a second gas of argon.

Yamazaki et al. teach forming the first f film or target silicon nitride but fail to teach that the formation is done using monosilane or disilane gas and nitrogen.

Kihira et al. teach forming a silicon nitride using monosilane or disilane gas and nitrogen. See col. 19, lines 20-25.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the silicon nitride as taught by Kihira et al. to obtain a stable silicon nitride at a low temperature. See col. 19, lines 20-25.

Further with respect to claim 72, Yamazaki et al. appear to fail to teach forming a thin film transistor over a substrate, wherein the thin film transistor comprises an active region and a gate electrode with a gate insulating film interposed therebetween.

However, the formation of a thin film transistor over a substrate, wherein the thin film transistor comprises an active region and a gate electrode with a gate insulating film interposed therebetween is well-known.

Further with respect to claims 34 and 39, Yamazaki et al. further teach forming a thin film transistor over a substrate, wherein the thin film transistor comprises of an active region and a gate electrode with a gate insulating film interposed therebetween. See fig. 1A.

With respect to claims 38 and 46, Yamazaki et al. further teach forming an EL layer 201 and an electrode 200 or 202 over the silicon nitride film 204. See fig. 4A.

With respect to claims 3, 11, 36, 44, 67, and 76, Yamazaki et al. fail to teach the substrate is made of glass or plastic material.

However, the formation of semiconductor devices on glass or plastic substrate is well-known.

With respect to claims 4, 12, 37, 45, 68, and 77, Yamazaki et al. teach forming the silicon nitride protective film by sputtering but fail to teach that the target silicon nitride film is formed by plasma CVD.

However, the formation of silicon nitride by plasma CVD is well-known.

With respect to claims 2, 10, 35, 43, 66, and 75, Yamazaki et al. fail to teach the range for the formation pressure of forming the silicon nitride.

However, it would have been obvious to one of ordinary skill in the art of

making semiconductor devices to determine the workable or optimal value or range for formation pressure through routine experimentation and optimization to obtain optimal or desired device performance because it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claims 5, 14, and 70, Yamazaki et al. further teach forming a semiconductor device using the silicon nitride film as a protective film of a semiconductor element. See cols. 25 and 26 and associated figures.

With respect to claims 6, 15, and 71, Yamazaki et al. further teach that the semiconductor element is a thin film transistor. See fig. 1A and associated text.

Further with respect to claims 1, 7, 15, 34, 39, 63, and 72, Yamazaki et al. ('162) in combination with Kihira et al. teach the second film by sputtering but fail to teach that the first film is formed by CVD and the sputtering and CVD processes are performed in the same chamber to form the first and second films.

Fukui et al. teach forming a plurality of films by CVD and sputtering in the same chamber to prevent exposure to unwanted oxidative atmosphere. See the abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Fukui et al. into the process of Yamazaki ('162) and Kihira et al. to attain the above benefit.

Further with respect to claims 1, 7, 34, 39, 63, and 72, as currently amended, Yamazaki et al. teach forming the second film on the substrate using the first film as a target but fail to teach the the target film or first film is located a metal support or electrode.

Danek et al. teach locating a target film over an metal support or electrode in chamber to provide current or potential to the target film to provide the deposition of target material. See para [0114].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Danek et al. to attain the above benefit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP